DETAILED ACTION

1. This communication is responsive to Amendment filed 04/10/2008.

2. Claims 2-5 and 7-26 are pending in this application. Claims 12, 15, 21, and 26 are independent claims. In Amendment, claims 1 and 6 are cancelled and claim 26 is added. This Office Action is made final.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 2-5 and 7-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 2-5 and 7-26 cite a processor and method for performing FFT in accordance with a mathematical algorithm. However, claims 2-5 and 7-26 merely disclose steps/components for performing FFT without disclosing a practical/physical application. Therefore, claims 2-5 and 7-26 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 12-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeh (U.S. 2004/0059766).

Re claim 12, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of N samples (e.g. abstract and Figure 3 wherein the input is either x(n)/X(N) depending on the processed of FFT/IFFT respectively), the processor comprising:

at least one FFT triplet module (e.g. part 37 in Figure 3), the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output data sequence in accordance with a butterfly operation performed on the input data sequence (e.g. 31a and 8 in Figure 3), the first stage radix-2 butterfly unit having a first feedback memory connected thereto;

a second FFT stage having a selectable multiplier for selectively multiplying the first stage output data sequence by a trivial coefficient, wherein a selectable multiplier is selected in response to a first control signal provided by a first control circuitry with the second FFT stage module (e.g. Figures 3 and 5 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), and a second stage radix-2 butterfly unit controlled by the switching signal and providing a second stage output data sequence in accordance

with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto (e.g. part 32 and 4 in Figure 3); and

a third FFT stage having a multiply selectable multiplier for selectively multiplying the second stage output data sequence by at least one of the trivial coefficient and a complex coefficient, wherein a selectable multiplier is selected in response to a second control signal provided by a second control circuitry with the third FFT stage module (e.g. Figures 3 and 6 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the multiply selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence (e.g. part 33 and 2 in Figure 3) (e.g. wherein each of the stage of BF is clearly addressed or shown in Figures 4-6 respectively).

Re claim 13, Yeh further discloses in Figures 1-16 each of the first, second and third stage output data sequences X(k,n) is equal to $x(n)+(-1)^k x(n+N/2)$ (e.g. inverse processed in BFII of Figure 9).

Re claim 14, Yeh further discloses in Figures 1-16 at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial coefficient multiplication to a received input data sequence (e.g. Figure 9 with BFII and BFIII).

Re claim 15, Yeh discloses in Figures 1-16 a pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of N samples (e.g. triplet 37 in Figure 3 and the abstract wherein the input data sequence is either x(n)/X(N) depending on the processed FFT/IFFT respectively), the processor comprising:

at least one FFT triplet module (e.g. triplet 37 in Figure 3), the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output data sequence in accordance with a butterfly operation performed on the input data sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto (e.g. BFI 31a and 8 in Figure 3);

a second FFT stage having a multiply selectable multiplier for selectively multiplying the first stage output data sequence by at least one of the trivial coefficient, wherein a selectable multiplier is selected in response to a first control signal provided with the second FFT stage module (e.g. Figures 3 and 5 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the first control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), and a second stage radix-2 butterfly unit responsive to the current switching signal for providing a second stage output data

sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto (e.g. BFII 32 and 4 in Figure 3); and

a third FFT stage having a selectable multiplier for selectively multiplying the second stage output data sequence by a trivial coefficient, wherein a selectable multiplier is selected in response to a second control signal provided with the third FFT stage module (e.g. Figures 3 and 6 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10), a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence (e.g. part 33 and 2 in Figure 3) (e.g. wherein each of the stage of BF is clearly addressed or shown in Figures 4-6 respectively).

Re claim 16, Yeh further discloses in Figures 1-16 each of the first, second and third stage output data sequences X(k,n) is equal to $x(n)+(-1)^k x(n+N/2)$ (e.g. inverse processed in BFII of Figure 9).

Re claim 17, Yeh further discloses in Figures 1-16 at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial coefficient multiplication to a received input data sequence (e.g. Figure 9 with BFII and BFIII).

Re claim 18, Yeh further discloses in Figures 1-16 an FFT terminator determined in accordance with the length N of the input data sequence (e.g. either Figure 3 or Figure 10).

Re claim 19, Yeh further discloses in Figures 1-16 the FFT terminator includes a butterfly module having a memory sized to store a single sample, for receiving as a terminator input, the output of the third FFT stage multiplier and for performing a butterfly operation on the terminator input to render an FFT of the input data sequence of N samples (e.g. as with the BFI as seen in Figure 3).

Re claim 20, Yeh further discloses in Figures 1-16 the FFT terminator includes a first butterfly module having a memory sized to store a pair of samples, for receiving as a terminator input, the output of the third stage multiplier and for performing a butterfly operation on the terminator input (e.g. Figures 4-6), and a second butterfly module connected to the first butterfly module of the terminator by a selectable multiplier, the selectable multiplier for selectively multiplying the output of the first butterfly module of the terminator by -j, the second butterfly module having a memory sized to store a single sample and for performing a butterfly operation on the selectively multiplied output of the first butterfly module of the terminator to render an FFT of the output data sequence (e.g. as with the BFI and BFII as seen in Figure 10 and its corresponding Figure 11A).

Re claim 21, Yeh discloses in Figures 1-16 Yeh discloses in Figures 1-16 a method of performing an FFT on a data sequence of N samples in an FFT processor having a butterfly module (e.g. Figure 3 and abstract), the method (e.g. for purposes of illustration Figures 2-3 are used to illustrate the features of prior art) comprising: for all

integers x according to 1.ltoreq.x.ltoreq.log.sub.2N (e.g. there are 16 input data label as X[0] to X[15]), repeating the steps of receiving and buffering $N/2^x$ samples at a time from a data sequence having N samples (e.g. sampling and initialization), generating a 2-point FFT using the n.sup.th and the 24 (n + N 2 x) the samples (e.g. X[0] and X[8] are computed together); selectively multiplying the generated 2-point FFT data sequence by a complex valued multiplicand (e.g. as seen in Figure 2 only the last four data are multiplied with j); wherein a multiplier is selected in response to a control signal provided with each butterfly module (e.g. Figures 3 and 5-8 wherein the base butterfly operation is seen in Figure 4 with add and subtract routing signals), the control signal comprising a combination of a current and a prior switching signal (e.g. by the control unit 36 in Figure 3 or control unit 606 in Figure 10); terminating the FFT using a termination data sequence determined in accordance with a (log.sub.2N)mod3 relationship to obtain an FFT of the sequence of N samples; and outputting the FFT of the sequence of N samples (e.g. Figure 3 or Figure 10).

Re claim 22, Yeh further discloses in Figures 1-16 the complex valued multiplicand is selected from a list including 1, - j , sqrt(2)/2 - jsqrt(2)/2 ,and a complex twiddle factor coefficient (e.g. Figures 3-6).

Re claim 23, Yeh further discloses in Figures 1-16 (log.sub.2N)mod3=1 and the step of terminating the FFT includes buffering a sample received from the final selective multiplication and performing a 2-point FFT using the buffered sample and the subsequent sample in the data sequence to obtain the FFT of the data sequence of N samples (e.g. as with the BFI as seen in Figure 3).

Re claim 24, Yeh further discloses in Figures 1-16 (log.sub.2N)mod3=2 and the step of terminating the FFT (e.g. Figures 4-6) includes: buffering a pair of samples received from the final selective multiplication and performing pair-wise 2-point FFTs using the two buffered samples and the two subsequent samples in the data sequence; selectively multiplying the result of the pair-wise 2 point FFT by –j (e.g. Figures 4-6 as butterfly component for BFI, BFII, and BFIII); and buffering a sample received from the selective multiplication of the pair-wise 2-point FFT and performing a 2-point FFT using the buffered sample and the subsequent sample in the data sequence to obtain the FFT of the data sequence of N samples (e.g. as with the BFI and BFII as seen in Figure 10 and its corresponding Figure 11A).

Re claim 25, Yeh further discloses in Figures 1-16 an FFT terminator determined in accordance with the length N of the input data sequence (e.g. either Figure 3 or Figure 10).

Response to Arguments

7. Applicant's arguments filed 04/10/2008 have been fully considered but they are not persuasive.

a. The applicant argues in page 10 second paragraph for claims rejected under 35 U.S.C. 101 that the claims disclose a method of performing an FFT on a data sequence of N samples in an FFT processor having a butterfly module.

The examiner respectfully submits that the claims merely disclose a series of mathematical/mental steps or components for performing FFT wherein the

butterfly module, as just another mathematical operation, is a mathematical part of the FFT operation. Thus, the whole claims direct to a mathematical operation on the samples as FFT.

b. The applicant argues in page 11 last paragraph to page 12 for independent claims 12, 15, and 21 that the cited reference fails to disclose a corresponding control signal which comprises a combination of a current and prior switching signal.

The examiner respectfully submits that the above alleged limitation is logically seen in the cited reference by Yeh, particularly paragraphs [0059, 0063, 0074 and 0084] wherein the IFFT control unit generates corresponding control signals to the butterfly modules. Since the claims do not specific how the combination is made between the current and previous, the cited portions broadly meet the claimed limitation. Each of the control signals is generated based upon the value of the step-count registers wherein the step-count value is based upon the combination (e.g. in this case, the addition) of the cycle bit as current value and the previous value of the step-count register as previous value.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Chat C. Do/
Primary Examiner, Art Unit 2193

June 4, 2008